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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/753,326
Filing Date: December 29, 2000
Appellant(s): KEDIA ET AL.

Gordon R. Lindeen III
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed December 10, 2007 appealing from the Office action mailed August 31, 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6240521	Barber et al.	5-2001
5287485	Umina et al.	2-1994
5768164	Hollon, Jr.	6-1998
6108663	Kabelshkov	8-2000

5983073	Ditzik	11-1999
5590197	Chen	12-1996

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 29, 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Umina et al., US Patent 5287485, hereinafter Umina, in view of Barber et al., US Patent 6240521, hereinafter Barber.

3. In re claim 29, Umina discloses a method comprising [fig.2; col.4, ll. 14-20]:

- A computer system having a CPU [202] and a memory [204].
- A [low power] subsystem including a [low power] processor [206] and a [low power] memory [208].

4. Umina did not disclose low power operations associated with the dual processors configuration with separate memories.

5. Barber discloses a method comprising:

- Transitioning a central processing unit (CPU) [high speed processor 42] of a computer system [40] into a low power mode [sleep] [col.4, ll.4-12], the computer system having a memory [50, RAM, DISK, fig.2] [col.3, ll.36-52].

- Activating a low power subsystem [44 with associated components] when the CPU enters the low power mode, the low-power subsystem including a low power processor [44] and an external interface [48] [col.4, ll.13-22].
- Independent of the CPU, using the low power processor of the low power subsystem to access data [contents of memory associated with process state] within the computer system memory [col.2, ll.13-19; col.3, ll.36-52; col.4, ll.13-22; 44 accesses data such as word processing from computer system memory while 42 is in sleep mode inactive].
- Providing the accessed data [e.g., word processing] through the external interface of the low-power subsystem [col.2, ll.13-19; word processing requires user interaction via well known monitor and keyboard conventionally through 48].

6. It would have been obvious to one of ordinary skill in the art, having the teachings of Barber and Umina before him at the time the invention was made, to modify the system taught by Umina to include the low power operations taught by Barber, as both are involved with dual processors [e.g., Barber's computer system memory 50 would be analogous to Umina's 204]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to conserve power and integrate processors with different capabilities [Barber: col.2, ll.13-29].

7. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Umina and Barber as applied to claims 29, 38 and 51 above, and further in view of Kableshkov, US Patent 6108663.

8. Umina and Barber taught each and every limitation as discussed above in reference to claims 29, 38 and 51. Umina and Barber did not discuss the details of accessing data.

9. In re claim 30, Kabelshkov discloses a method wherein accessing data comprises accessing data through a shared database [relational database of 31] of a low power subsystem [30], the method further comprising storing at least a partial copy of data accessed from a computer system [10] memory [34] in the shared database [col.4, ll.36-61].

10. It would have been obvious to one of ordinary skill in the art, having the teachings of Kabelshkov, Umina and Barber before him at the time the invention was made, to incorporate the teachings of Kabelshkov as the shared database taught by Kabelshkov is well known to be suitable for use in the system of Umina and Barber. One of ordinary skill in the art would have been motivated to make such a combination as it provides an efficient way to access data [Kabelshkov: col.4, ll.50-56].

11. Claims 38-40, 42, 44, 48-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Hollon", US Patent 5768164, in view of Umina.

12. In re claim 38, Hollon discloses an apparatus [10] comprising:

- A computer system [i.e., associated with active mode] having a central processing unit [81], a system memory [82], and a user interface [e.g., 20], the computer system having a low power mode [inactive] [fig.1; col.3, l.2].
- A low-power subsystem [i.e., associated with inactive mode] in operation when the computer system enters the low power mode, the low power subsystem having a low power processor [84] and an external interface [e.g., 39] independent of the computer system, the low power processor providing access to the computer system when the computer system is in the low power mode and the external interface providing data accessed from the computer system externally [col.3, ll. 1-17].

13. Hollon did not disclose explicitly a mass storage device and a low power subsystem memory.

14. Umina discloses an apparatus [fig.2] comprising a computer system having a CPU [202] and a system memory [204]; a [low power] subsystem having a [low power] processor [206] and a [low power] subsystem memory [208].

15. It would have been obvious to one of ordinary skill in the art, having the teachings of Hollon and Umina before him at the time the invention was made, to modify the system taught by Hollon to include the additional memories of a mass storage device and a subsystem memory for the low power subsystem, as the use of mass storage devices and other memories for additional storage capacity is well known in the art. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to increase memory capacity and access flexibility [i.e., adding memory enables more information to be stored; separate subsystem memory for low power subsystem enables local storage for access flexibility].

16. In re claim 51, Hollon discloses a low-power subsystem [col.1, ll.21-29; col.3, ll.1-5; a subsystem with main system 10 and main display 20 inactive is relatively low-power] comprising:

- A miniature display screen [39].
- A user input unit [94 or 31-38].
- A low-power processor [84, 92 and associated components processes user inputs and displays outputs] coupled to the miniature display screen and the user input unit, the low power processor providing access for the miniature display screen and the user input unit to a connected computer system when the computer system is in a low power mode

[inactive] [col.2, l.51 – col.3, l.5; col.3, ll.23-67; 82 contains applications shared when 10 is active or inactive].

17. Hollon did not disclose explicitly a low power subsystem memory.

18. Umina discloses an apparatus [fig.2] comprising a computer system having a CPU [202] and a system memory [204]; a [low power] subsystem having a [low power] processor [206] and a [low power] subsystem memory [208].

19. It would have been obvious to one of ordinary skill in the art, having the teachings of Hollon and Umina before him at the time the invention was made, to modify the system taught by Hollon to include the additional memories of a subsystem memory for the low power subsystem. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to increase memory capacity and access flexibility [i.e., adding memory enables more information to be stored; separate subsystem memory for low power subsystem enables local storage for access flexibility].

(10) Response to Argument

A. Claim 29 is obvious where the references teach or suggest "using the low power processor of the low power subsystem to access data contained within the computer system memory."

Applicant's individualistic analysis of the references does not clarify the rejection based on combination. Examiner briefly presents the main point of the rejection based on Umina in view of Barber:

In re claim 29, Umina discloses a method comprising [fig.2; col.4, ll. 14-20]:

- A computer system having a CPU [202] and a memory [204].

- A [low power] subsystem including a [low power] processor [206] and a [low power] memory [208].

However, Umina did not disclose low power operations. In other words, Umina discloses the main structural components, including operations such as using one processor [206] to access data within the computer system memory [204] during normal operation, but did not discuss other operation modes such as low power operation. Thus, Examiner provided Barber, which also discloses a dual processor system, to disclose the low power operation:

- Transitioning a central processing unit (CPU) [high speed processor 42] of a computer system [40] into a low power mode [sleep] [col.4, ll.4-12], the computer system having a memory [50, RAM, DISK, fig.2] [col.3, ll.36-52].
- Activating a low power subsystem [44 with associated components] when the CPU enters the low power mode, the low-power subsystem including a low power processor [44] and an external interface [48] [col.4, ll.13-22].
- Independent of the CPU, using the low power processor of the low power subsystem to access data [contents of memory associated with process state] within the computer system memory [col.2, ll.13-19; col.3, ll.36-52; col.4, ll.13-22; 44 accesses data such as word processing from computer system memory while 42 is in sleep mode inactive].
- Providing the accessed data [e.g., word processing] through the external interface of the low-power subsystem [col.2, ll.13-19; word processing requires user interaction via well known monitor and keyboard conventionally through 48].

It would have been obvious to one of ordinary skill in the art, having the teachings of Barber and Umina before him at the time the invention was made, to modify the system taught

by Umina to include the low power operations taught by Barber, as both are involved with dual processors [e.g., Barber's computer system memory 50 would be analogous to Umina's 204]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to conserve power and integrate processors with different capabilities [Barber: col.2, ll.13-29].

Applicant argues that "neither reference shows a whole subsystem", but does not point out which ***claimed*** limitation relating to the subsystem is missing from the ***combined*** references. Examiner submits that Barber discloses explicitly at least a low power subsystem [44 with associated components] including a low power processor [44] and an external interface [48] while Umina discloses subsystems each having their own memories.

Applicant argues that "'using the low power processor of the low power subsystem to access data contained within the computer system memory'... in Barber, there is only one memory, while in Umina, there is no low power subsystem". Examiner submits that the rejection based on ***combination*** shows that one with ordinary skill in the art, not an automaton, would find it obvious to incorporate Barber's low power operation mode associated with dual processors into Umina's own dual processors system in order to conserve power consumption.

Applicant argues that "'providing the accessed data through the external interface of the low-power subsystem'... is not possible with either reference as there is no separate external interface for the second processor". It is not apparent how the claim distinguishes the "***separate***" external interfaces. Examiner submits that Barber discloses providing the accessed data through the external interface [48] of the low-power subsystem.

Applicant argues that "neither reference shows a low power subsystem, only a second processor". Examiner disagrees and submits that Barber discloses explicitly at least a low power subsystem [44 with associated components] including a low power processor [44] and an external interface [48] while Umina discloses subsystems each having at least their own memories.

Applicant argues that "such a modification of Umina then goes against the teachings of Umina and reduces its performance for the reasons that Umina provides". Examiner disagrees and submits that Applicant's support, cited from Umina's column 1, lines 50-65, are directed to ***prior art*** of which Umina strives to improve upon. In other words, Umina's actual invention in figure 2 would have no teachings against incorporating modifications associated with Barber's low power operations.

Applicant argues that "Examiner could have argued that it would be obvious to apply the dual memory/dual processor system of Umina to the high power/low power system of Barber..." Examiner did not make such rejection, but submits that adding a second memory space to Barber would not have defeat the shared address space because Barber did not teach against transferring data other than the current machine state [e.g., working data] seamlessly from the computer system memory to the added second memory space.

As demonstrated, Umina and Barber ***combined*** clearly teach each and every limitation.

B. Claim 30 is obvious where the references teach or suggest "a shared database with at least a partial copy of [the] data."

Applicant argues that "Kabelshkov does not show a shared database... has no low power mode" Examiner disagrees and submits that Kabelshkov does disclose a method wherein

accessing data comprises accessing data through a shared database [relational database of 31] [col.4, ll.50-61]. Additionally, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. In the instant case, Kabelshkov's teachings to efficiently access data would be applicable to many systems, including the low power subsystem of Barber.

C. Claims 38 and 51 are obvious when the reference suggests "a low power subsystem memory" and providing access to a connected computer system when the connected computer system is in a low-power mode'"

Applicant argues that Hollon "mentions power consumption as an issue in the Background... however, Hollon does not address the problem..." Examiner finds it illogical and unreasonable that Hollon would mention power consumption as an issue in the Background and then ignore the problem. Examiner submits that Hollon addresses power consumption by at least disclosing an inactive mode [col.3, l.2]. One with ordinary skill in the art would know that laptops such as Hollon's conserve power by going into inactive modes when the lids are closed.

Applicant argues that "at least the main CPU 81... must all be operating... only CPU in the system". Examiner disagrees as Applicant's mere conclusory remarks have no support. Furthermore, Examiner submits that Applicant's logic makes no sense as to why Hollon would include an ASIC to operate when the laptop lid is closed, if the CPU is to be active and can perform all operations [CPUs are general processors whereas ASIC are processors customized for specific tasks such as operations during inactive mode].

Applicant argues that "spontaneous use display mode will actually increase power consumption". Examiner disagrees with the mere conclusory remark and finds it questionable that Hollon would raise the power consumption issue and then propose a solution to exacerbate the problem.

Applicant argues that "Umina has two memories but these are shared by the two processors... neither memory can be assigned to either processor". Firstly, Examiner agrees with Applicant's concession that Umina's memories are shared by the two processors as the concession shows that Umina does disclose independent of a CPU, using a [low power] processor of a [low power] subsystem to access data with the memory of the CPU. This concession would further strengthen Examiner's rejection of claim 29 in showing that Umina already teaches this operation, except when in low power operation mode [i.e., taught by Barber]. Secondly, Examiner submits that Umina does show that each of the memories is assigned to their respective processor [col.4, ll.14-20]. Applicant appears to suggest that the memories are to be exclusive in access by their respective processors, to which Examiner submits that such access-exclusion features are not explicitly claimed nor enabling disclosed.

Applicant argues that "there is no access to the computer system when it is in low-power mode in either reference". Examiner disagrees and submits that at least Hollon discloses accessing the computer system when it is in low-power [inactive] mode in order to run the applications in the spontaneous use display [col.2, l.51 – col.3, l.5; col.3, ll.23-67; 82 contains applications shared when 10 is active or inactive].

Applicant argues that "adding a low power subsystem to Hollon... significantly increase complexity..." Examiner is not aware of any evidence that would suggest one with ordinary skill

in the art, not an automaton, would have considered adding memory to be complex in view of the particular references.

Applicant argues that "there is nothing in Umina to suggest adding a redundant memory and display from Hollon". Examiner did not make such rejection, but is perplexed as to why Umina would add a redundant memory when Umina already teaches dual memories.

As demonstrated, Umina and Hollon ***combined*** clearly teach each and every limitation.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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1/22/08

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